From event structures theory to weak memory models

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PPLV Seminar

Message-passing on my computer

Consider this program `mp`:

$$\begin{array}{c} \texttt{data} = \texttt{flag} = 0 \\ \texttt{data} := 17; \;\|\; r \leftarrow \texttt{flag}; \\ \texttt{flag} := 1 \;\|\; \texttt{if}(r == 1)\{v \leftarrow \texttt{data}\} \end{array}$$

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Possible execution traces on my computer:

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Message-passing on my phone

$$
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$$

Possible execution traces on my **phone**:

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- $\mathtt{R}_{\texttt{flag}=0} \cdot \mathtt{W}_{\texttt{flag}:=1} \cdot \mathtt{W}_{\texttt{data}:=17}$

A different **architecture**, much harder to reason about ...

Structure behind traces

$$\begin{cases} \mathtt{W_{flag}{:=}1} \cdot \mathtt{W_{data}{:=}17} \cdot \mathtt{R_{flag}{=}1} \cdot \mathtt{R_{data}{=}17} \\ \mathtt{W_{flag}{:=}1} \cdot \mathtt{R_{flag}{=}1} \cdot \mathtt{W_{data}{:=}17} \cdot \mathtt{R_{data}{=}17} \\ \mathtt{W_{data}{:=}17} \cdot \mathtt{W_{flag}{:=}1} \cdot \mathtt{R_{flag}{=}1} \cdot \mathtt{R_{data}{=}17} \end{cases}$$

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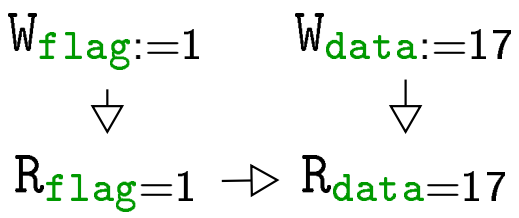

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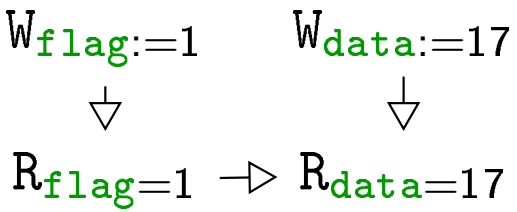
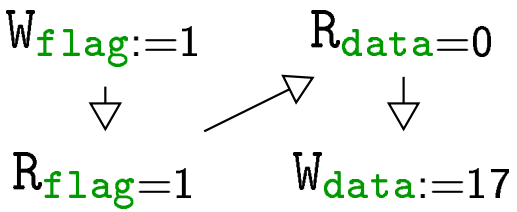


$$\{ \quad \mathtt{W}_{\mathtt{flag}:=1} \cdot \mathtt{R}_{\mathtt{flag}=1} \cdot \mathtt{R}_{\mathtt{data}=0} \cdot \mathtt{W}_{\mathtt{data}:=17}$$



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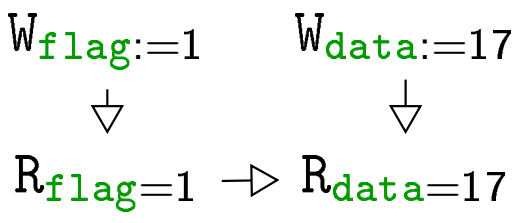

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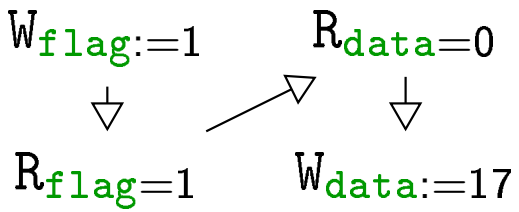

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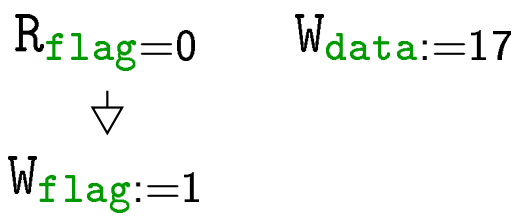

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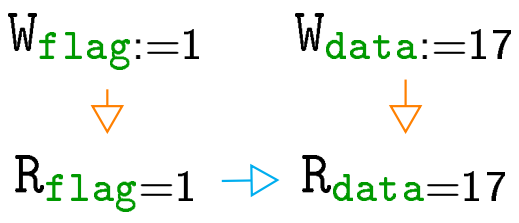
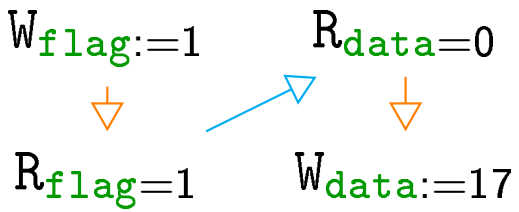


$$\{ \quad \mathtt{W}_{\mathtt{flag}}{:=}1 \cdot \mathtt{R}_{\mathtt{flag}}{=}1 \cdot \mathtt{R}_{\mathtt{data}}{=}0 \cdot \mathtt{W}_{\mathtt{data}}{:=}17$$



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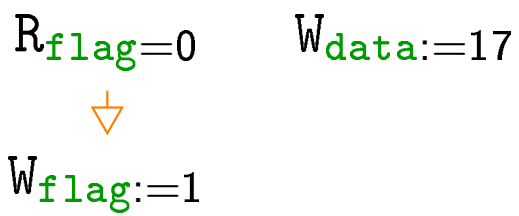
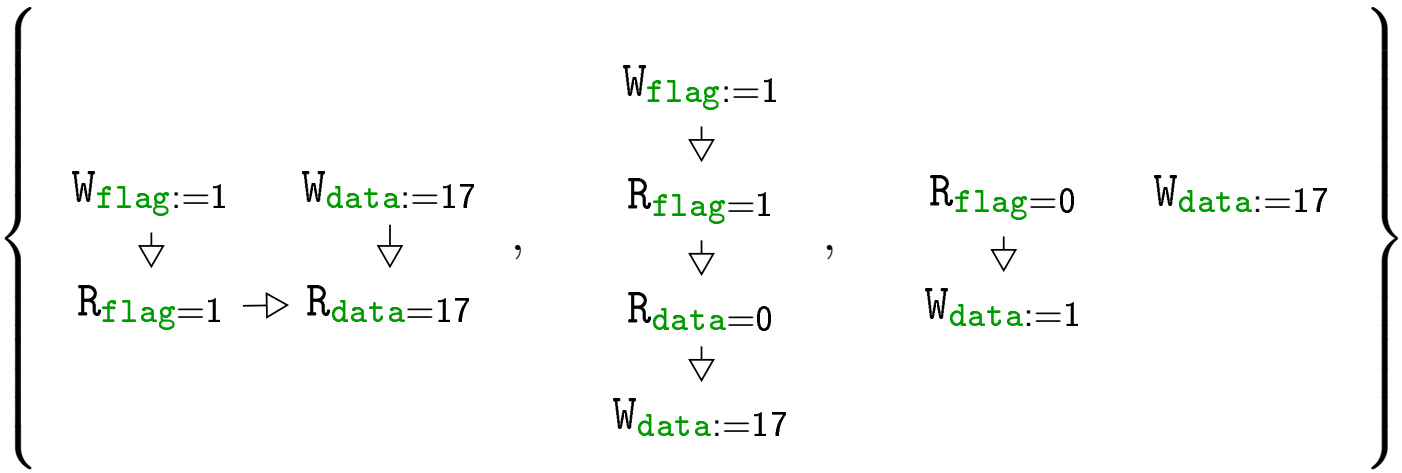


Sets of partial orders and event structures

The **set of partial orders** describes the semantics of `mp`:



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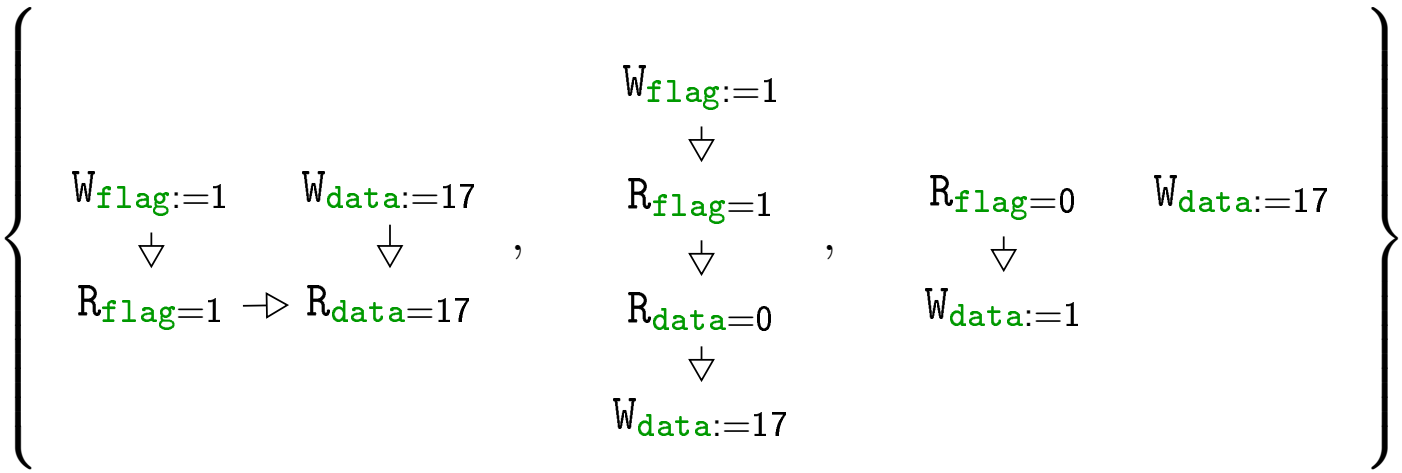
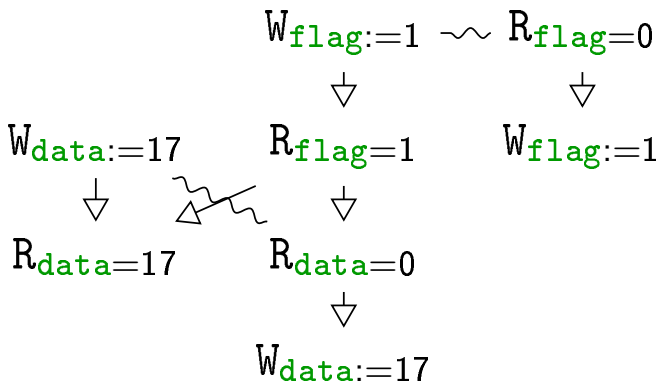


This set of partial orders can be summed by an **event structure**:



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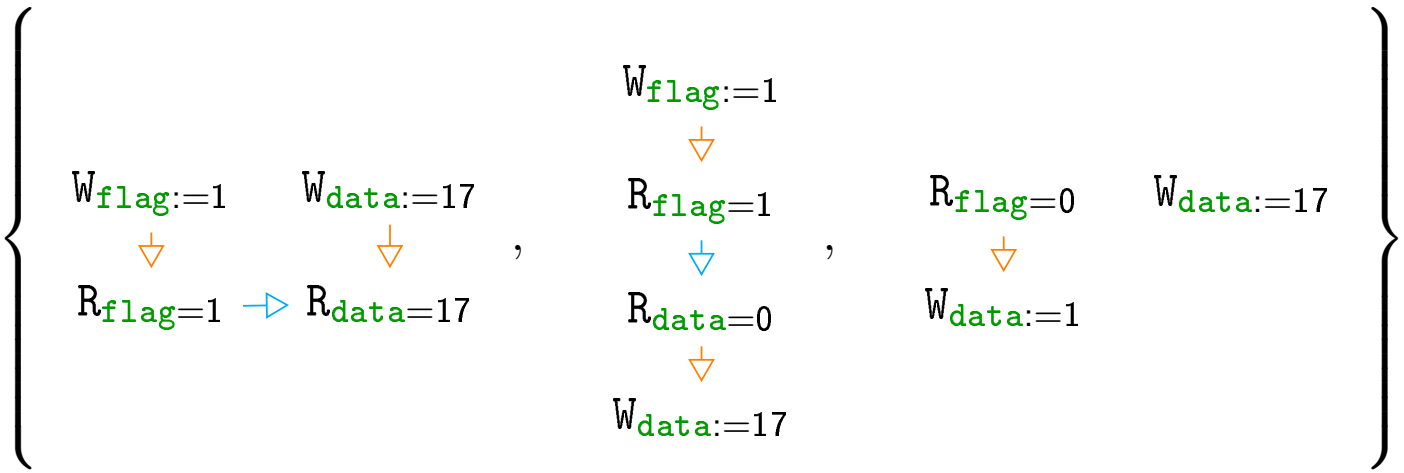

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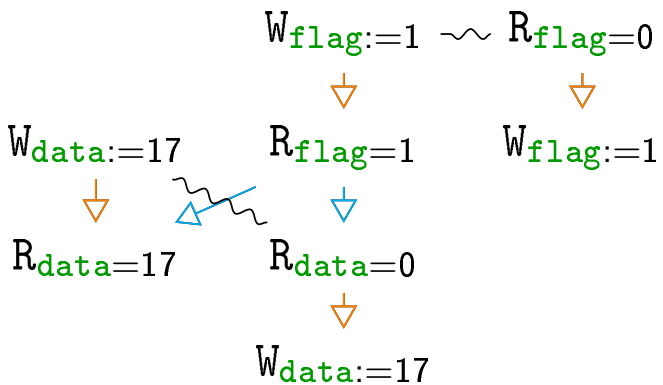

This talk

1. **A semantics for threads, and a semantics for memory**
2. **Using theory to mix them.**
3. **Applications to theory and practice.**

I. A semantics for threads, and a semantics for memory

Modelling MiniARM

MiniARM: An assembly language with relaxed semantics

Syntax. Idents split in thread-local registers and global variables.

$$e ::= r \mid e + e \mid \dots$$
$$t ::= \texttt{fence}; t \mid \texttt{x} := e; t \mid r \leftarrow \texttt{x}; t$$
$$p ::= t \parallel \dots \parallel t$$

Actions. We observe the following actions from the programs:

$$\Sigma ::= \mathtt{W}_{\texttt{x}:=k} \mid \mathtt{R}_{\texttt{x}=k} \mid \texttt{fence}.$$

Semantics. Described by a labeled transition system on states p, μ:

$$\langle p \mathbin{@} \mu \rangle \xrightarrow{\ell \in \Sigma} \langle p' \mathbin{@} \mu' \rangle. \qquad (\mu, \mu' : \texttt{Var} \to \mathbb{N})$$

It is **relaxed**: operations on independent variables can be reordered.

A few rules

Thread rules: $\langle t \mathbin{@} \mu \rangle \xrightarrow{\ell} \langle t' \mathbin{@} \mu' \rangle$:

$$\frac{}{\langle \mathtt{x} := k; t @ \mu \rangle \xrightarrow{\mathtt{W}_{\mathtt{x}:=k}} \langle t @ \mu[\mathtt{x} := k] \rangle}$$

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$$\frac{\langle t @ \mu \rangle \xrightarrow{\ell} \langle t' @ \mu' \rangle \qquad \ell \neq \mathtt{fence} \qquad \mathtt{var}(\ell) \neq \mathtt{x}}{\langle \mathtt{x} := k; t @ \mu \rangle \xrightarrow{\ell} \langle \mathtt{x} := k; t' @ \mu' \rangle}$$

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$$\frac{\langle t @ \mu \rangle \xrightarrow{\ell} \langle t' @ \mu' \rangle \qquad \ell \neq \mathtt{fence} \qquad \mathtt{var}(\ell) \neq \mathtt{x}}{\langle \mathtt{x} := k; t @ \mu \rangle \xrightarrow{\ell} \langle \mathtt{x} := k; t' @ \mu' \rangle}$$

And then:

$$\frac{\langle t_i \mathbin{@} \mu \rangle \xrightarrow{\ell} \langle t_i' \mathbin{@} \mu' \rangle}{\langle t_1 \parallel \ldots \parallel t_i \parallel \ldots \parallel t_n \mathbin{@} \mu \rangle \xrightarrow{\ell} \langle t_1 \parallel \ldots \parallel t_i' \parallel \ldots \parallel t_n \mathbin{@} \mu' \rangle}$$

Operational traces and memory states

These rules generates the **operational (partial) traces**:

$$\mathrm{Tr}(p, \mu) = \{\ell_1 \dots \ell_n \mid \langle p \mathbin{@} \mu \rangle \xrightarrow{\ell_1} \dots \xrightarrow{\ell_n} \langle p' \mathbin{@} \mu' \rangle\}.$$

From, there we can compute the final memory states:

$$\mathsf{MemStates}(p) = \{\mu(t) \mid t \in \mathrm{Tr}(p, (\mathtt{x} \mapsto 0)) \text{ is a maximal trace}\}.$$

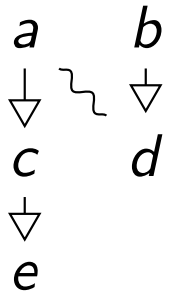
where $\mu(t) = \mathtt{x} \mapsto$ last value written to $\mathtt{x}$ or zero.

$: \mathcal{V} \to \mathbb{N}$

Labeled event structures

Definition

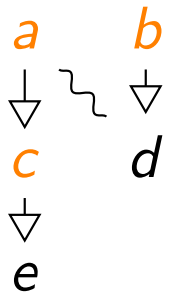
A (Σ-labeled) **event structure** is a tuple $(E, \leq_E, \sharp_E, \ell : E \to \Sigma)$ where $(E, \leq_E)$ is a partial order and $\sharp_E$ is a symmetric relation on E, satisfying *finite causes* and *conflict inheritance*.



Labeled event structures

Definition

A (Σ-labeled) **event structure** is a tuple $(E, \leq_E, \sharp_E, \ell : E \to \Sigma)$ where $(E, \leq_E)$ is a partial order and $\sharp_E$ is a symmetric relation on E, satisfying *finite causes* and *conflict inheritance*.



- **Configurations** are downclosed, conflict-free subsets of E. $\mathscr{C}(E)$ is the set of configurations of E.

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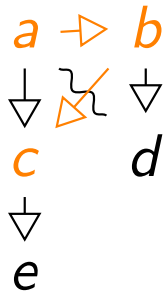


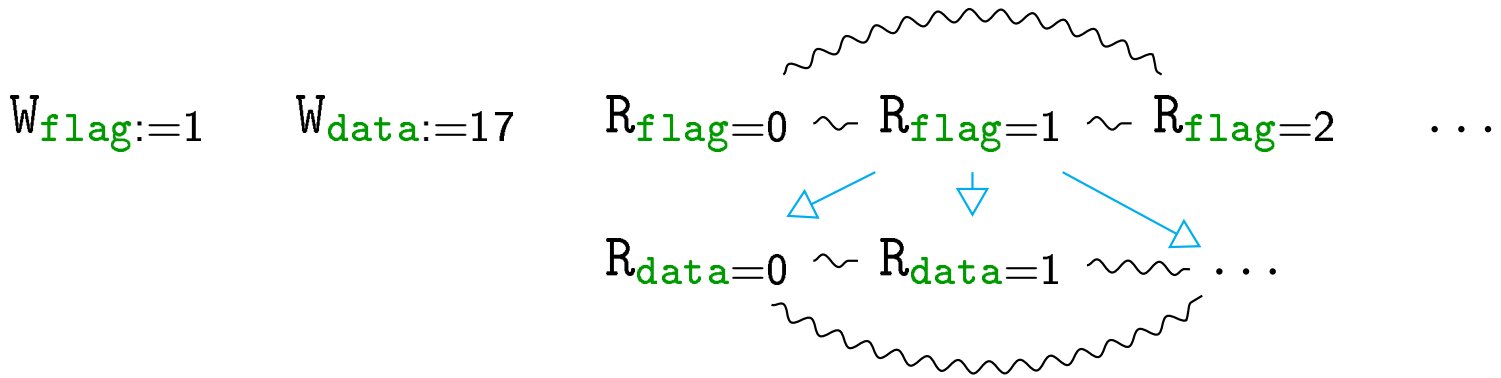
- **Configurations** are downclosed, conflict-free subsets of E. $\mathscr{C}(E)$ is the set of configurations of E.
- A **trace** of E is a linearisation of a configuration of E. $\mathrm{Tr}(E)$ is the set of traces of E (can be seen as a subset of Σ^*).

Our goal: a mapping $[\![\cdot]\!]$ from states to event structures s.t.:

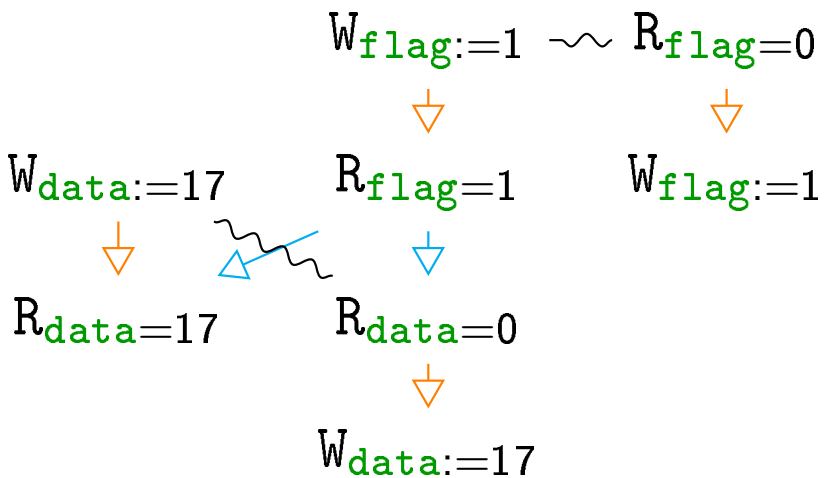
$$\mathrm{Tr}(p, \mu) = \mathrm{Tr}[\![p, \mu]\!].$$

An overview of the semantics

1. **Thread semantics**: context is left open (and unknown)



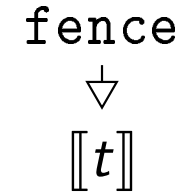
2. **Final semantics**: context is assumed empty
   Compute interactions with memory:



Thread semantics

Fences. $[\![\texttt{fence}; t]\!] = \texttt{fence} \cdot [\![t]\!]$

$(\leq_{\ell \cdot E} = \leq_E \cup \{(\ell, \ell')\})$



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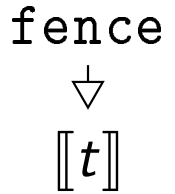

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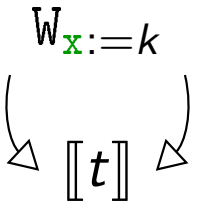

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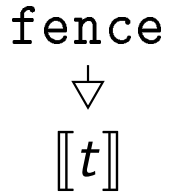

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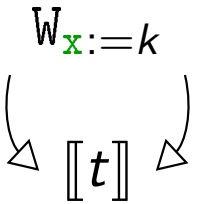

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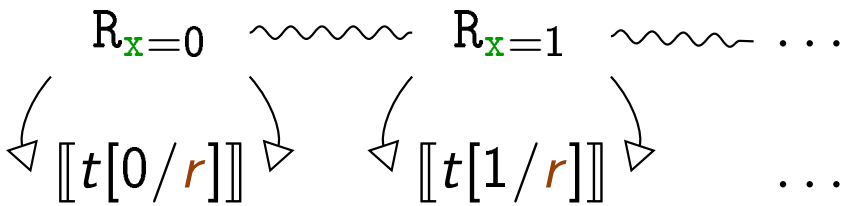

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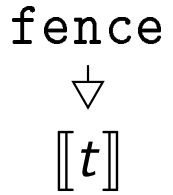

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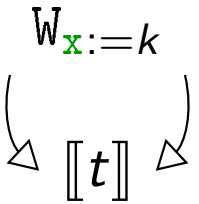

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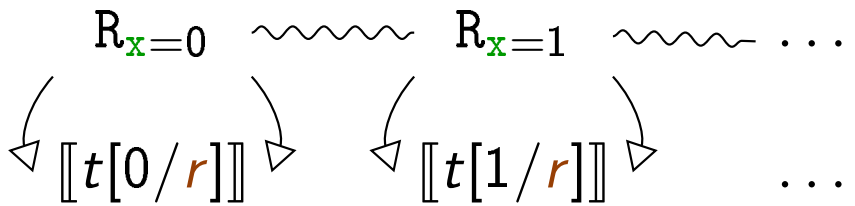

Program. No interaction: $[\![t_1 \parallel \ldots \parallel t_n]\!] = [\![t_1]\!] \parallel \ldots [\![t_n]\!]$.

Wiring memory behaviour

The memory behaviour is specified through **consistent traces**:

$$C_\mu ::= \mathtt{W}_{\mathtt{x}:=k} \cdot C_{\mu[\mathtt{x}:=k]} \mid \mathtt{fence} \cdot C_\mu \mid \mathtt{R}_{\mathtt{x}=\mu(\mathtt{x})} \cdot C_\mu$$

Theorem

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But I promised an e.s. $[\![p, \mu]\!]$! (**causally** account for memory)

Causal account for the memory

$\rightsquigarrow$ Instead of a set of *traces* C_μ, a set of *partial orders* $\mathscr{C}_\mu$.

No canonical notions, but several compromises:

Definition

A partial order **q** is:

- **semantically consistent** when $\mathrm{Tr}(\mathbf{q}) \subseteq C_\mu$.
- **syntactically consistent** when for each variable `x`, actions in **q** on `x` are linearly ordered.

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$$\mathscr{C}_\mu^{\mathsf{sem}} = \{\mathbf{q} \mid \mathbf{q} \text{ semantically consistent}\}.$$
$$\mathscr{C}_\mu^{\mathsf{syn}} = \{\mathbf{q} \mid \mathbf{q} \text{ syntactically consistent}\}.$$

We have $\mathrm{Tr}(\mathscr{C}_\mu^{\mathsf{sem}}) = \mathrm{Tr}(\mathscr{C}_\mu^{\mathsf{syn}}) = C_\mu$ but $\mathscr{C}_\mu^{\mathsf{sem}} \subsetneq \mathscr{C}_\mu^{\mathsf{syn}}$.

II. Event structure theory

How to merge $[\![p]\!]$ and $\mathscr{C}_\mu$

Briding a gap: event-based and execution-based models

ES

$[\![p]\!]$

Briding a gap: event-based and execution-based models

$\mathbf{ES}$ $\qquad\qquad$ $\mathrm{Set}(\mathbf{PO})$

$[\![p]\!]$ $\qquad\qquad$ $\mathscr{C}_\mu$

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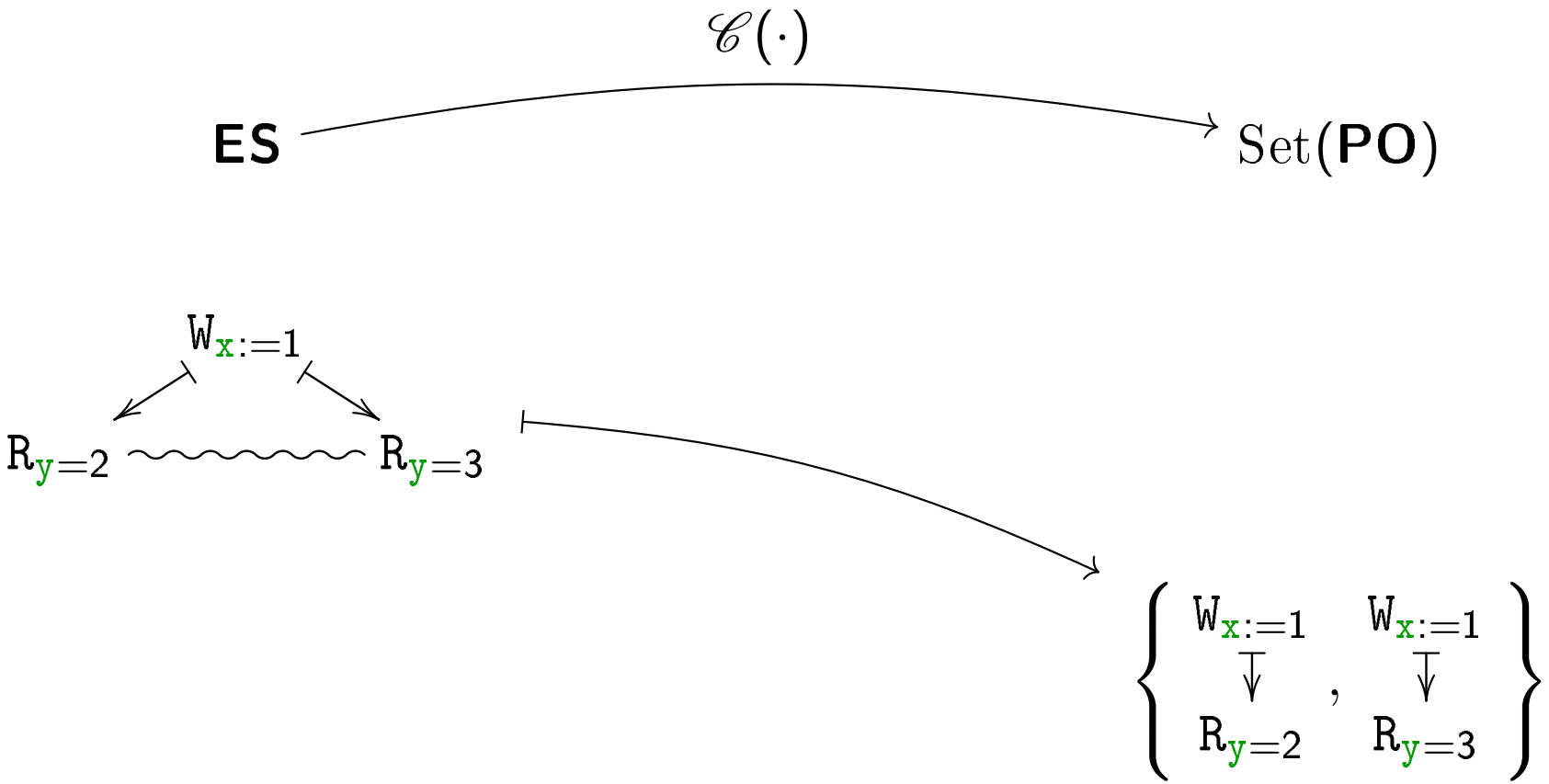

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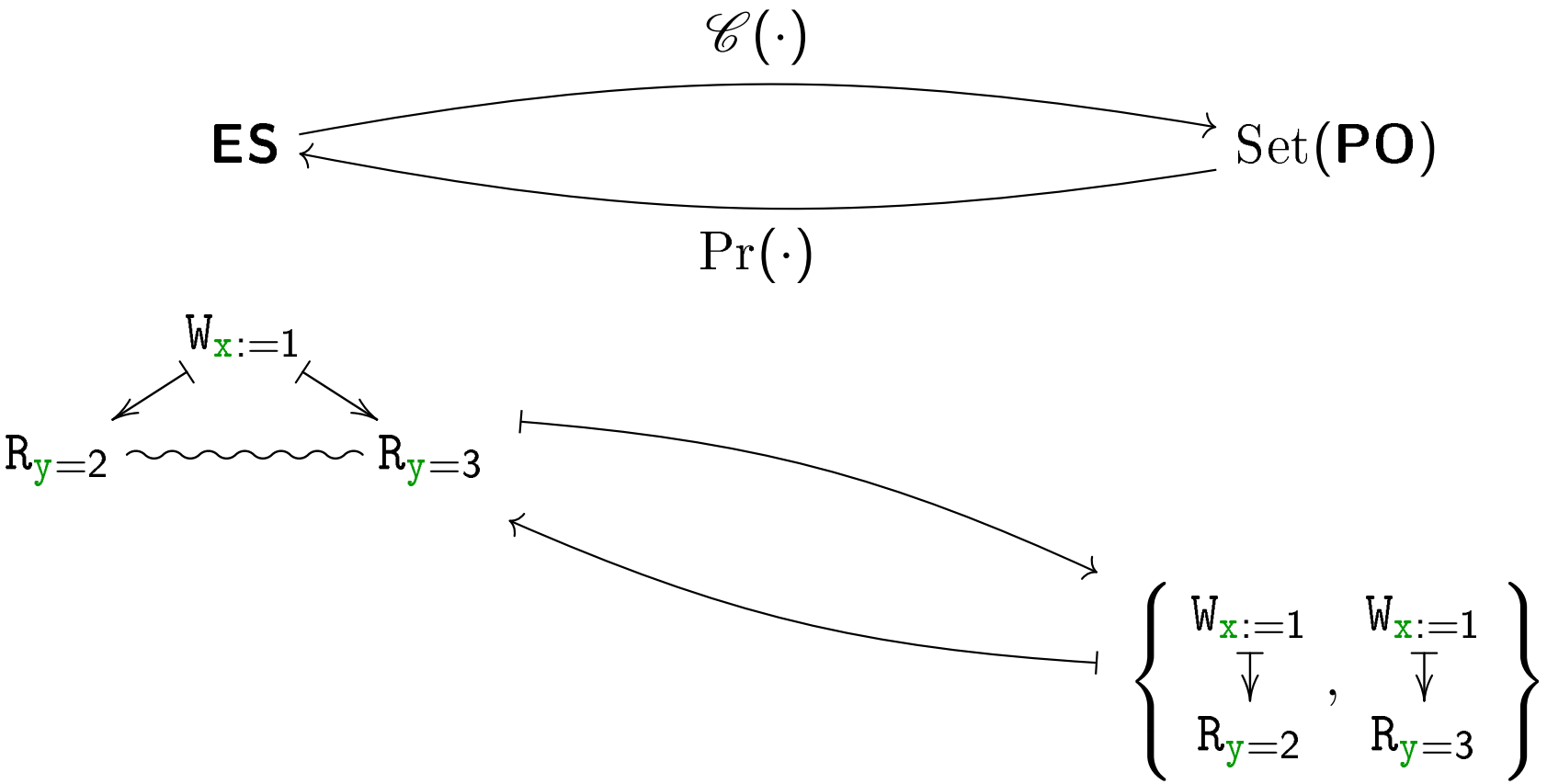

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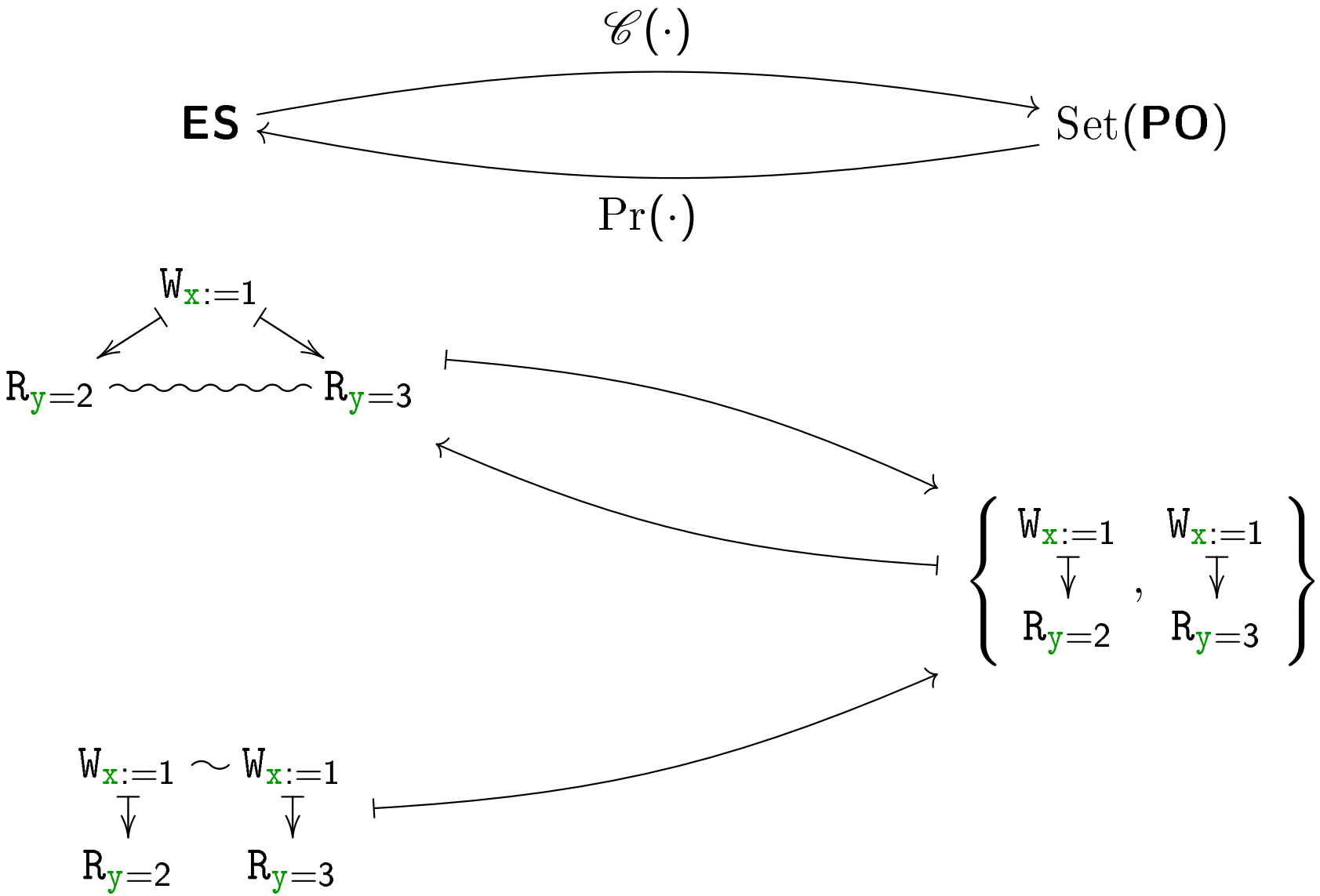

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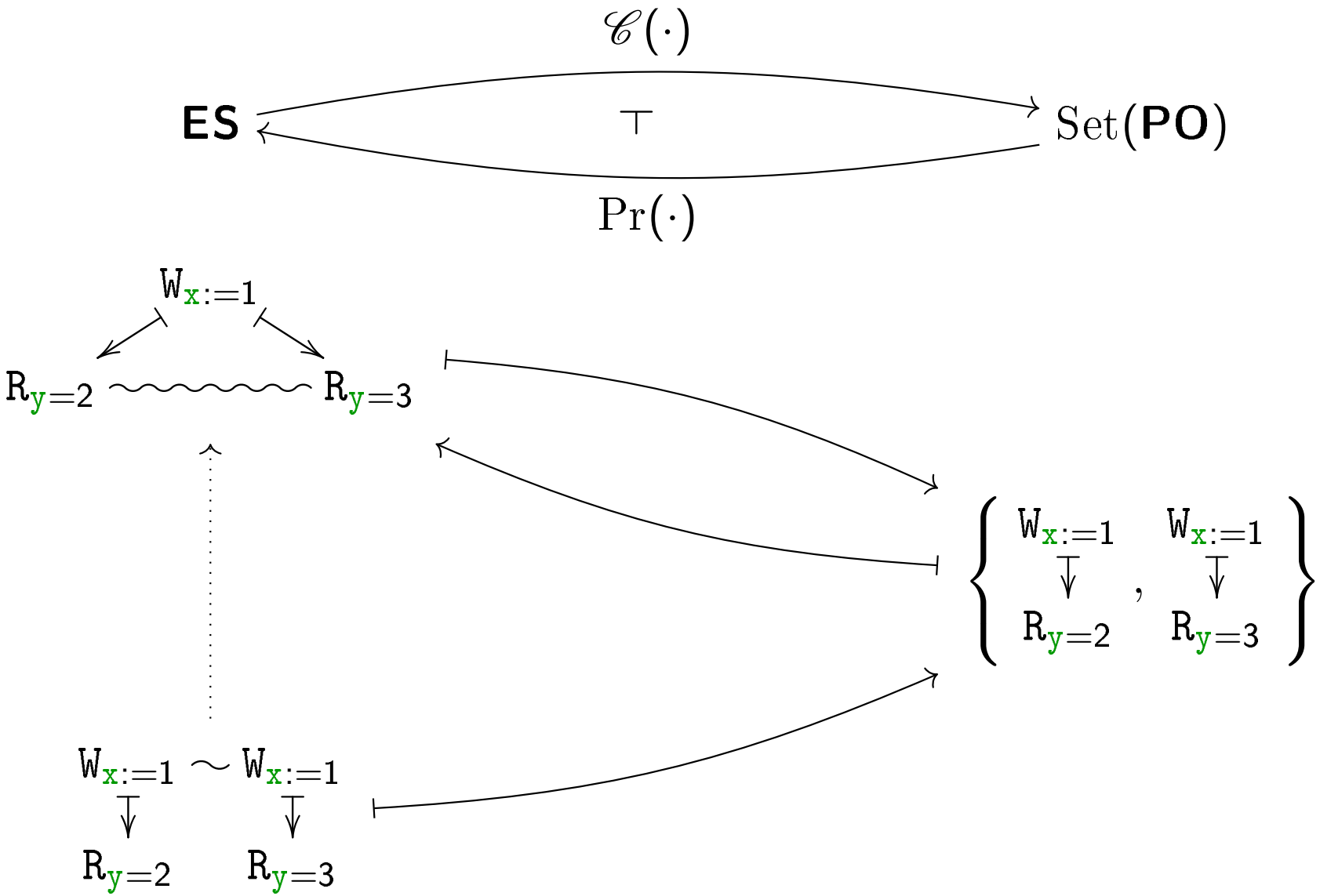

The prime construction: details

Consider a set $\mathscr{Q} \in \mathrm{Set}(\mathbf{PO})$ *closed under prefix*. We define $\mathrm{Pr}(\mathscr{Q})$:

Events Those $\mathbf{q} \in \mathscr{Q}$ with a top element

Causality $\mathbf{q} \leq \mathbf{q}'$ when $\mathbf{q}$ is a prefix of $\mathbf{q}'$

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NB: $\mathscr{C}(\mathrm{Pr}(\mathscr{Q})) \cong \mathscr{Q}$.

A partial product on partial orders

Given two partial orders $\leq_{\mathbf{q}}, \leq_{\mathbf{q}'}$ on the same carrier set, write:

$$\mathbf{q} \wedge \mathbf{q}' = \begin{cases} (\mathbf{q} \cup \mathbf{q}')^* & \text{if a partial order} \\ \text{undefined} & \text{otherwise} \end{cases}.$$

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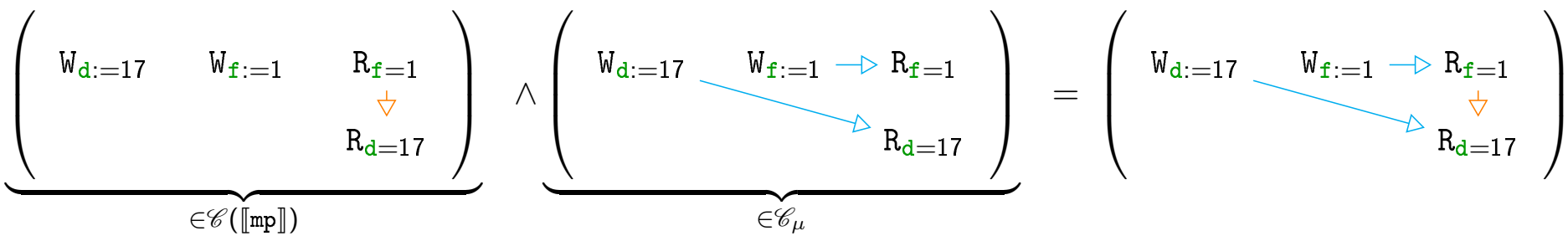

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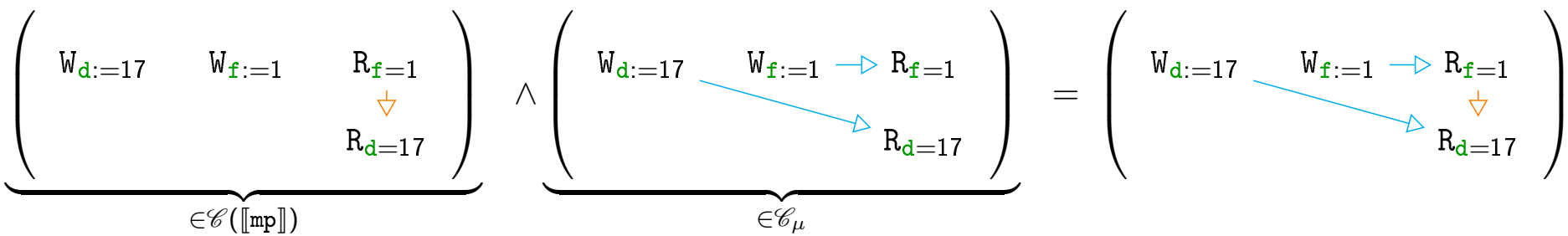

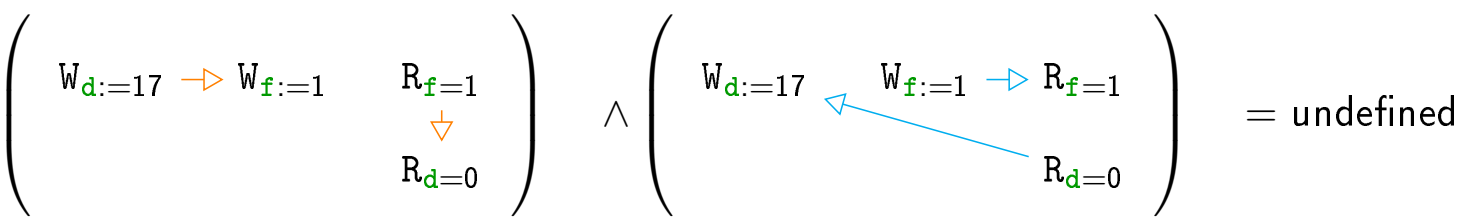

$= \text{undefined}$

. . . generating a product on event structures

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$$P{*}Q = \{p \wedge q \mid p \in P, q \in Q\}.$$

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Theorem

Both operations are categorical products.

Note:

$$\mathrm{Tr}(E{*}E') = \mathrm{Tr}(E) \cap \mathrm{Tr}(E')$$

Illustrations of this construction

- Conflicts are merged:

$$\left(\begin{array}{ccc} a \sim b & & c \end{array} \right) * \left(\begin{array}{ccc} a & & b \sim c \end{array} \right) = \left(\begin{array}{ccc} a \sim b \sim c \end{array} \right)$$

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$$\begin{pmatrix} a \rightsquigarrow b & c \end{pmatrix} * \begin{pmatrix} a & b \rightsquigarrow c \end{pmatrix} = \begin{pmatrix} a \rightsquigarrow b \rightsquigarrow c \end{pmatrix}$$

- Events with incompatible histories are duplicated:

$$\begin{pmatrix} a \rightsquigarrow a & b \end{pmatrix} * \begin{pmatrix} a \\ \downarrow \\ b \end{pmatrix} = \begin{pmatrix} a \rightsquigarrow a \\ \downarrow \quad \downarrow \\ b \quad b \end{pmatrix}$$

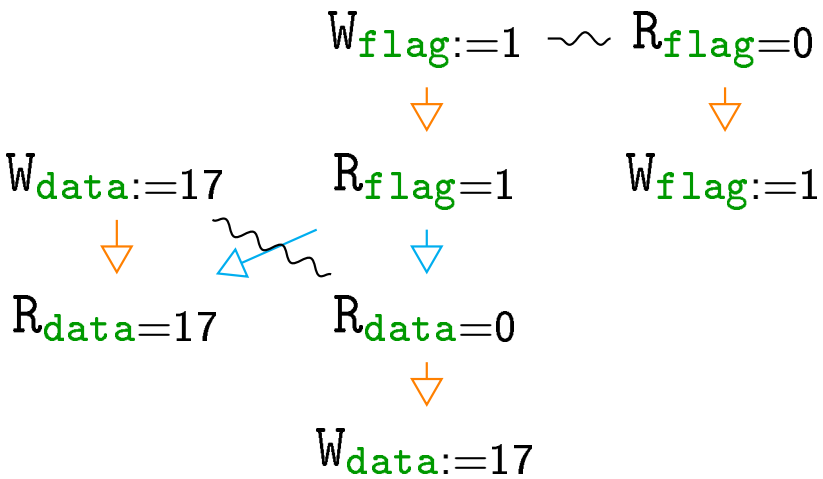
A final model

Define $[\![p, \mu]\!]^{\mathsf{mem}} = \Pr(\mathscr{C}([\![p]\!]) * \mathscr{C}_\mu^{\mathsf{mem}})$. We have:

$$\mathrm{Tr}[\![p, \mu]\!]^{\mathsf{mem}} = \mathrm{Tr}[\![p]\!] \cap \mathrm{Tr}[\![\mathscr{C}_\mu^{\mathsf{mem}}]\!] = \mathrm{Tr}[\![p]\!] \cap C_\mu = \mathrm{Tr}(p, \mu).$$

Yields the desired result:

$[\![\mathtt{mp}, (\mathtt{x} \mapsto 0)]\!]^{\mathsf{syn}} =$



III. Applications

(1) Theory: Data racefreedom
(Joint work with Jade Alglave and Jean-Marie Madiot)

Races and sizes

A race: two co-located concurrent accesses (among which a write).

$$\texttt{data} := \texttt{0xdeadbeef} \;\Big\|\; \begin{array}{l} r \leftarrow \texttt{data} \\ \texttt{assert}\ (\texttt{data} \in \{0, \texttt{0xdeadbeef}\}) \end{array}$$

If data is two words, we might see: $\texttt{data} = \texttt{0xdead0000}$.

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If `data` is two words, we might see: $\texttt{data} = \texttt{0xdead0000}$.

But, `mp` should be ok:

$$\begin{array}{l} \texttt{data} := 17; \\ \texttt{flag} := 1 \end{array} \;\Big\|\; \begin{array}{l} r \leftarrow \texttt{flag}; \\ \texttt{if}(r == 1)\{v \leftarrow \texttt{data}\} \end{array}$$

The race on `flag` does not matter since `flag` is "small".

"Small locations" and the notion of race

To model this, we split variables into two groups:

`multi word variables` `single word variables`.

Races on single words variables are ok (necessary to implement eg. locks).

Definition

A **race** of a program p is a a trace $w \in (\mathbb{N} \times \Sigma)^*$ of the form:

$$w = \ldots \cdot (i, \mathtt{R}_{\mathtt{x}=k}) \cdot (j, \mathtt{W}_{\mathtt{x}:=k'})$$

with $i \neq j$ and `x` is a multi word variable.

Definition

A program is **well-synchronized** (or **race-free**) when none of its traces *on SC* are races.

Data-Racefreedom

A wanted property for most architectures:

Definition (Data Racefreedom (DRF))

An architecture $\mathcal{A}$ satisfies (DRF) when for all well-synchronized program p,

$$\mathsf{MemStates}_{\mathsf{SC}}(p) = \mathsf{MemStates}_{\mathcal{A}}(p).$$

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Theorem

Our architecture MiniARM satisfies data racefreedom.

Proof.

In two steps:

1. Show that if p is race-free *on MiniARM*, then $\mathsf{MemStates}_{\mathsf{SC}}(p) = \mathsf{MemStates}_{\mathcal{A}}(p)$.
2. If p has a race on MiniARM, then it has a race on SC. □

III. Applications

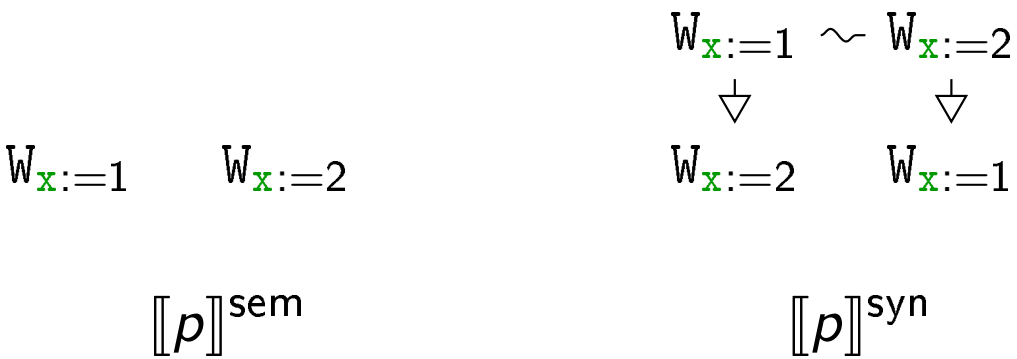
(2) Practice: smaller structures
(Joint work with Jade Alglave and Jean-Marie Madiot)

Two different compromises

- $\mathscr{C}_\mu^{\mathsf{sem}}$ is too hard to compute (check **all** the traces)
- $\mathscr{C}_\mu^{\mathsf{syn}}$ is too big (forces linearisation on each variable)

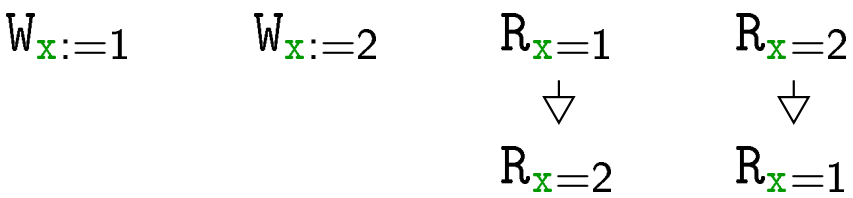
$\rightsquigarrow$ Can we do better? Not force all writes to be synchronized.

$$\mathtt{x} := 1 \;\|\; \mathtt{x} := 2$$



Observing order

Consider:



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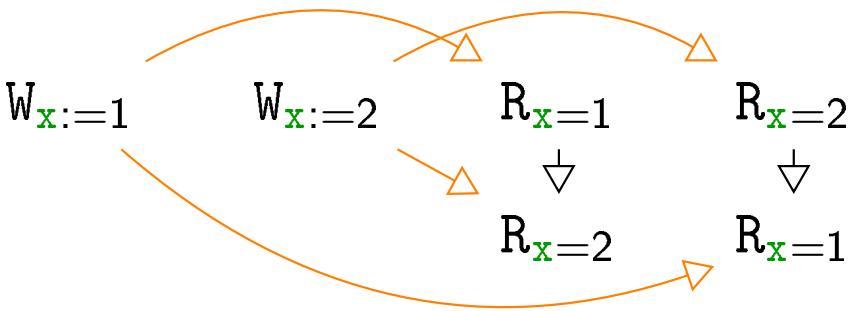
Consider:



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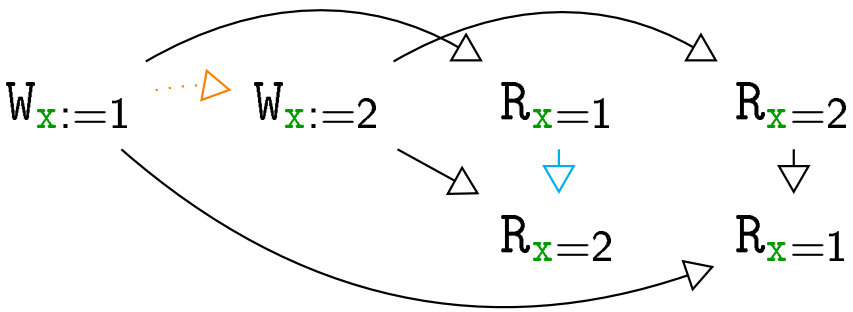

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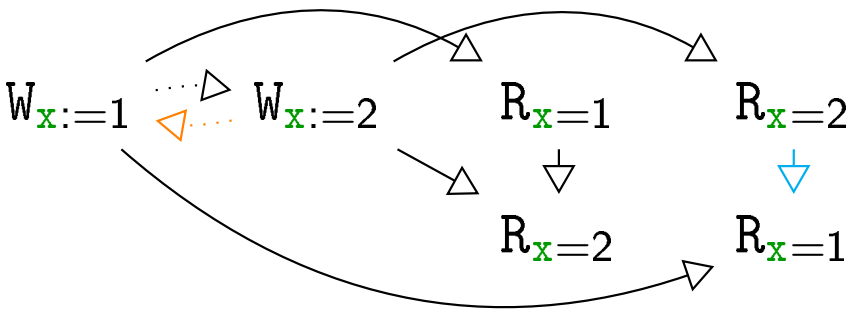

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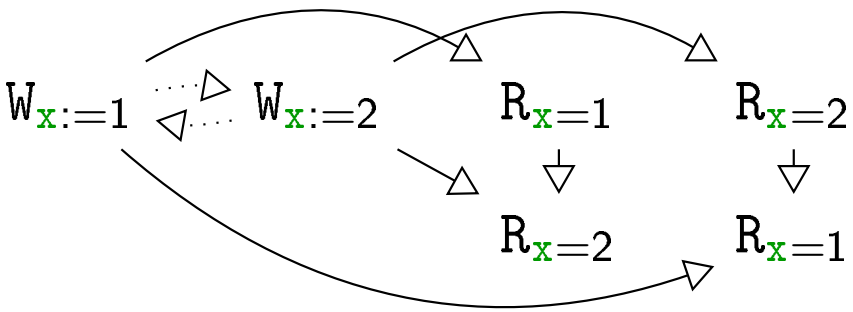

By investigation, we find a set of axioms...

Lazy consistency

Definition

A partial order $\mathbf{q}$ is **lazily consistent** when it satisfies:

- For every read $r_x \in \mathbf{q}$, there exists a (unique) maximal write $\mathrm{just}(w_x)$ below r_x, with the same value.
- If whenever $w_x : \mathtt{W}_{\mathtt{x}:=\_} \leq r_y : \mathtt{R}_{\mathtt{y}=\_}$ and $w_y : \mathtt{W}_{\mathtt{y}:=\_} \leq r_x : \mathtt{R}_{\mathtt{x}=\_}$ with $\mathrm{just}(r_x) \neq w_x, \mathrm{just}(r_y) \neq w_y$, then $w_x < \mathrm{just}(r_x)$ or $w_y < \mathrm{just}(r_y)$ (or possibly both).

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Theorem (**Weaker correctness**)

Up to permutations of reads and independent writes, every trace of a lazy consistent po is consistent.

$\rightsquigarrow \mathrm{MemStates}([\![p]\!]^{\mathsf{lazy}}) = \mathrm{MemStates}(p)$.

A demo

$$P = \quad \texttt{x} := 1 \;\Big\|\; \texttt{x} := 3$$

$$Q = \quad \begin{array}{c|c|c} \texttt{x} := 1 & \texttt{x} := 3 & r \leftarrow \texttt{x} \\ & & s \leftarrow \texttt{x} \end{array}$$

Related work / Extensions

Related work.

- Brookes et al.'s model of TSO with pomsets.
- Pichon et al.'s operational semantics on event structures
- Jeffrey and Riely's axiomatic model using event structures

Extensions. Extend this to:

- Real ARM, TSO, Linux-C, etc.
- More complicated C11 models.